REMARKS

INTRODUCTION

In accordance with the foregoing, no claims have been amended. Claims 1-15 are pending and under consideration.

CLAIM REJECTIONS – 35 USC 102

Claims 1 and 4-8 were rejected under 35 USC 102(b) as being anticipated by Becerra et al. (US 5,917,509) (hereinafter "Becerra").

Becerra discloses a method and apparatus for interleaving pulses in a liquid recorder. Becerra discloses a thermal ink jet printhead 68, a power supply source 66 and a system controller 67. The thermal ink jet printhead 68 is activated by two pulses which are interleaved in time and supplied to different emitter banks 96. One of the pulses is controlled by the corresponding data which is to be recorded. There are 128 emitters, organized into 32 emitter banks 96 of four emitters per bank. The electrothermal transducers 46 which cause the ink emission are electrically attached to a power supply source 66 via the burn voltage line 70. Each electrothermal transducer 46 is also attached to a power transistor 51 that switches the burn voltage 70 to ground through the transducer 46. Becerra, 6:15-6:29 and Figure 7.

A predriver circuit 74 provides the necessary gate voltage level to the power transistor 51 so that it will turn fully on. The predriver circuit 74 functions like a logical AND gate having logical inputs from a data line 94 and the emitter bank selection shift register 90. The predriver circuit 74 also serves as the interface between the low voltage logic circuitry and the higher voltage circuitry needed to apply power pulses to the electrothermal transducers 46. Becerra, 6:51-6:64 and Figure 7.

Further in Becerra, power pulsing of individual transducers 46 within an emitter bank 96 is controlled via an input to the predrivers 74 which are connected to the four data lines 94. A second input to the predrivers 74 is shared by all of the predrivers 74 of an emitter bank 96. There is provided a separate second predriver input line 92 for each of the 32 emitter banks 96 shown in the embodiment of FIG. 7. These second predriver input lines 92 are controlled by the bank selection shift register 90. The bank selection shift register 90 has 32 outputs, F1-F32, one for each emitter bank 96. When one of the output lines F1-F32 is logically high, the corresponding emitter bank 96 is able to be pulsed since the predrivers 74 of the corresponding bank are now able to close the corresponding power transistor switches 51 in response to

signals from the data lines 94. The bank selection shift register 90 functions to allow only one emitter bank 96 to be pulsed during any instant of time since the power source has been sized to accommodate only one emitter bank 96 at a time, to synchronize the selection of an emitter bank 96 with the proper set of 4 bits of data appearing on the data lines 94 for that bank 96, and to cycle through all of the emitter banks 96 so that there is an opportunity for every emitter to be activated by both PHASE B pulses and PHASE A pulses. The bank selection shift register 90 further provides for the interleaving of the pulses between the emitter banks 96 so that full cycling through all of the banks 96 for the two pulses can be accomplished much more rapidly than if the pulses were not interleaved. The bank selection shift register 90 is also bi-directional so that the selection of emitter banks 96 can proceed from the first bank to the last bank or vice versa. Becerra, 8:4-8:34 and Figure 7.

Still further in Becerra, a direction signal generator 88 provides to the bank selection shift register 90 the signals DIR N and DIR P. The direction signal generator 88 derives from the DATA/DIRECTION line 71 and FUNCTION CLEAR line 75 signals provided by the overall printer system controller 67. This signal establishes whether the bank selection shift register 90 will advance from emitter BANK 1 to emitter BANK 32 (DIR N, high; DIR P, low) or in the opposite direction from emitter BANK 32 to emitter BANK 1 (DIR N, low; DIR P, high). The DIR N/P state is set by the logical state of the DATA/DIRECTION line 71 at the time the FCLR makes its rising logic transition 121 shown on the timing diagram of FIG. 8 of Becerra. Until the next FCLR signal is sent by the printer system controller 67, the DATA/DIRECTION line 71 is used to shift in DATA as described above and the direction signal generator ignores the data signals on this shared line. The printer system controller 67 provides the proper direction signal at each FCLR rising logic transition 121. Becerra, 10:36-10:55 and Figures 7 and 8.

Claim 1

Claim 1 recites: "...generating and supplying data for determining simultaneous firing nozzles and a nozzle group firing direction through a fire/group direction data line..." In contrast to claim 1, Becerra does not disclose determining data for determining simultaneous firing nozzles. In Becerra, the overall system controller 67 provides circuitry with signals conveying data on line 71 and data bit shift shift clocking on 77, drop emission timing (ENABLE signals) on line 73, and logic circuit reset on line 75. Further in Becerra, the predrivers 74 receive logical inputs from the data lines 94. In Becerra, data for determining simultaneous firing nozzles and nozzle group firing direction is not through a fire/group direction data line as is recited in claim 1.

Withdrawal of the foregoing rejection is requested.

Claims 4-8

Claim 4 recites: "...a data processing unit which provides: input data comprising simultaneous firing nozzle data and data for determining a nozzle group firing direction..." In contrast to claim 4, Becerra does not disclose a data processing unit which provides simultaneous firing nozzle data and data for determining a nozzle group firing direction. In Becerra, a DATA/DIRECTION line 71 is used to shift in DATA and the direction signal generator ignores the data signals on this shared line. In Becerra, a printer system controller 67 provides the proper direction signal at each FCLR rising logic transition 121. A data processing unit as recited in claim 4 is not disclosed in Becerra.

Claims 5-8 depend on claim 4 and are therefore believed to be allowable for at least the foregoing reasons.

Withdrawal of the foregoing rejection is requested.

CLAIM REJECTIONS – 35 USC 103

Claims 2 and 3 were rejected under 35 USC 103(a) as being unpatentable over Becerra in view of Edelen et al. (US 6,547356) (hereinafter "Edelen").

Edelen discusses latching serial data in an ink jet print head.

Claims 2 and 3 depend on claim 1 and are therefore believed to be allowable for at least the foregoing reasons. Further, claims 2 and 3 patentably distinguish over Becerra and Edelen, taken alone or in combination. For example claim 3 recites ANDing the nozzle firing signals and the outputs of the nozzle group selection signals of the bi-directional shift register.

Withdrawal of the foregoing rejection is requested.

CLAIM REJECTIONS – 35 USC 103

Claims 9-15 were rejected under 35 USC 103(a) as being unpatentable over Becerra in view of Edelen and Morita et al. (US 6,511,160) (hereinafter "Morita").

Morita discusses a thermal ink-jet head and recording apparatus. In Morita, the 4-bit shift register 21 and the 32-bit bidirectional shift register 24 are reset by the FCLR signal. When these registers rise, the latch circuit 23 latches the DIR signal, whereby the shifting direction of the 32-bit bidirectional shift register 24 is determined. Then image data is output as the DAT/DIR signal and the BIT SHIFT signal is input as a clock signal for the 4-bit shift register 21. For example, the image data are sequentially taken into 4-bit shift register 21 when the BIT SHIFT

signal rises. When the 4-bit image data is taken in, it is latched in the latch circuit 22 when the ENABLE signal rises. The image data thus latched is fed into the AND circuit 25. Morita, 10:50-10:61 and Figure 13.

Claims 9-13

Claim 9 recites: "...a Y bit latch which latches the parallel Y bits in response to the latch clock..." In contrast to claim 9, Becerra disucusses providing a signal PHASE A as an output from timing generator circuit 86, which can also be presented to all of the logical OR gates 76. This PHASE A signal is not controlled by the data, but, if presented to the logical OR gates 76, will be passed out to all of the data lines 94. Therefore, in Becerra, the predrivers 74 receive logical inputs from the data lines 94 for either the case of PHASE B AND DATA being high (logically true) or PHASE A being high (logically true). The Y bit latch of Becerra does not latch the parallel Y bits in response to the latch clock as is recited in claim 9. This deficiency in Becerra is not cured by Edelen or Morita.

Claims 10-13 depend on claim 9 and are therefore believed to be allowable for at least the foregoing reason. Further, claims 10-13 patentably distinguish over Becerra, Edelen and Morita, taken alone or in combination. For example, claim 10 recites that the MSB and the LSB of the bi-directional shift are each initially preloaded with data of "1" prior to the values of the X parallel outputs being shifted.

Withdrawal of the foregoing rejection is requested.

Claims 14 and 15

Claim 14 recites: "...latching the parallel Y bits in response to a latch clock..." In contrast to claim 14, Becerra disucusses providing a signal PHASE A as an output from timing generator circuit 86, which can also be presented to all of the logical OR gates 76. This PHASE A signal is not controlled by the data, but, if presented to the logical OR gates 76, will be passed out to all of the data lines 94. Therefore, in Becerra, the predrivers 74 receive logical inputs from the data lines 94 for either the case of PHASE B AND DATA being high (logically true) or PHASE A being high (logically true). The Y bit latch of Becerra does not latch the parallel Y bits in response to a latch clock as is recited in claim 14. This deficiency in Becerra is not cured by Edelen or Morita.

Claims 15 depends on claim 14 and is therefore believed to be allowable for at least the foregoing reasons. Further, claim 15 patentably distinguishes over Becerra, Edelen and Morita, taken alone or in combination. For example claim 15 recites that outputting the X bits and an MSB and an LSB from the bi-directional shift register, and loading a 1 into each of the MSB and

the LSB and loading a 0 into each of the X bits as the predetermined value.

Withdrawal of the foregoing rejection is requested.

CONCLUSION

There being no further outstanding objections or rejections, it is submitted that the application is in condition for allowance. An early action to that effect is courteously solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

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Date: Nov 22, 2005

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